Check for updates

Computer Applications in Engineering Education

WILEY

SPECIAL ISSUE ARTICLE

An Open-Source SPICE Simulation Suite for Teaching the Memristor: Standard Inverter–OTA Emulator With Bloom-Aligned Laboratory Exercises

Fatih Gül

Department of Electrical and Electronics Engineering, Artificial Intelligence and Internet of Things Research Laboratory, Recep Tayyip Erdoğan University, Rize, Türkiye

Correspondence: Fatih Gül (fatih.gul@erdogan.edu.tr)

Received: 2 May 2026 | **Revised:** 15 September 2026 | **Accepted:** 25 September 2026

Keywords: engineering pedagogy | memristor emulator | open-source teaching tools | pinched hysteresis | SPICE simulation

ABSTRACT

The memristor—the fourth fundamental two-terminal circuit element—has become a key building block of neuromorphic computing, in-memory analogue arithmetic, and hardware-rooted security primitives. Despite this prominence in research, fabricated memristive devices remain inaccessible to most undergraduate teaching laboratories, and the topic is therefore typically restricted to symbolic exposition. This paper presents an open-source pedagogical packaging of the well-established CMOS-inverter + integrating-capacitor + OTA memristor emulator topology, adopted as is from several prior reports since 2014. The contribution is a turn-key teaching package: a single plain-text SPICE netlist that runs unmodified under the open-source ngspice and the freely distributed LTspice; a Python post-processing pipeline; a closed-form first-order model that predicts the hysteresis lobe area from the integrating capacitance, the transconductance and the excitation amplitude, giving instructors an analytic marking target; three laboratory exercises with assessment rubrics scaling along Bloom-taxonomy levels Remember → Apply → Analyse, differentiated into a second-year and a third-year track; and a public release under the MIT License. Over the 1 – 100 kHz band, the emulator satisfies all three of Chua's signatures quantitatively: the v–i locus is pinched at the origin to within 10^{-8} of the current amplitude, the lobe area decays as f^{-1} (measured log–log slope −1.000), and it grows as the cube of the excitation amplitude (slope +3.01). Measurements agree with the closed-form model to a constant 4.3% across four parameter sweeps. The package needs no licence, no fabricated device and no specialised CAD environment.

1 | Introduction

The memristor was postulated by Chua in 1971 as the missing fourth fundamental passive circuit element, complementing the resistor, capacitor and inductor through a constitutive relationship between charge and flux linkage [1]. The element remained largely a theoretical curiosity until 2008, when Strukov et al. reported a thin-film TiO_2 device whose behaviour matched Chua's prediction [2]. In the intervening years, memristive devices have become a central motif of modern electronics research: they underpin emerging non-volatile resistive random-access memory (RRAM) [3], analogue in-memory matrix-vector accelerators for deep neural networks [4], spiking-synapse implementations for neuromorphic processors [5], and hardware-intrinsic primitives such as physically unclonable functions for IoT security [6].

Despite this rapid maturation at the research frontier, memristive devices have not entered the undergraduate laboratory in any meaningful sense. Fabricated devices are not commercially packaged for educational use; their production requires thin-film deposition, lithography and characterisation infrastructure that lies far beyond the reach of a teaching budget. As a result, the memristor is still typically introduced at senior or graduate level—through symbolic exposition, with at most a brief look at a

All rights reserved, including rights for text and data mining and training of artificial intelligence technologies or similar technologies.

© 2026 Wiley Periodicals LLC.

published current–voltage trace—and students leave the course without ever interacting with the device's defining behaviour.

A natural way to bridge this gap is the use of a *behavioural emulator*: a small circuit, built only from textbook components, whose port behaviour reproduces the principal signatures of a memristor. Several such emulators have been proposed in the literature since 2014 [7–15], with increasing levels of fidelity and complexity. The topology adopted in the present work—a CMOS inverter followed by an integrating capacitor whose voltage controls the transconductance of an operational transconductance amplifier (OTA) driving the input port—has appeared in compact-CMOS form in Saxena [12], in extended logic-gate applications in Swaroop and Ahmad [13], in inverter-fed form in Poornima [14], and most recently in a current-mode OTA-based variant by Neifar et al. [15]. The present manuscript therefore makes no circuit-theoretic claim; the topology is adopted as is.

The contribution is an open-source pedagogical packaging of that standard topology, designed for direct deployment in undergraduate courses. The approach follows an established line of work in this journal: the integration of modelling and simulation into engineering education has been argued in detail by Magana and de Jong [16], and concrete realisations have been reported for the physics of P–N diodes [17], agile hardware development with an open-source engineering simulator [18], and a LabVIEW-driven photovoltaic-panel emulator paired with a teaching platform [19]. The present manuscript continues this line by adapting it, for the first time, to memristor circuit pedagogy. Specifically, we provide:

1. A single plain-text SPICE netlist (emulator.cir) that runs unmodified under the open-source ngspice and, with only the analysis directive changed, under the freely distributed LTspice, so that students on any operating system and any institutional license can reproduce numerically identical results from one shared source file;
2. A reproducibility-oriented set of post-processing scripts (Python 3 with NumPy and Matplotlib) that turn raw simulator output into the canonical figures students are expected to recognise: the pinched-hysteresis Lissajous figure, the frequency-dependent lobe collapse, and the lobe-area scaling laws;
3. A closed-form first-order relation between the integrating capacitance C_{in}, the transconductance G_0, the excitation amplitude V_0 and the hysteresis lobe area, derived in Section 3.1 and validated against simulation in Section 5.3. The relation gives instructors a quantitative marking target and gives students a predictable quantity, which is what makes the Analyse-level exercise assessable rather than merely descriptive;
4. Three laboratory exercises with assessment rubrics, scaling from observation to prediction, that map directly onto Bloom-taxonomy levels Remember → Apply → Analyse, each differentiated into a second-year and a third-year variant;
5. A public release of all source files under the MIT License, so that adoption by other institutions requires no licensing, no implementation effort, and no fabricated device.

The Supporting Information S1 accompanying this paper is organised as follows, so that a reader looking for a specific resource can go to it directly: SI-A is the ready-to-print handout for Laboratory Exercise 1 (hysteresis fingerprint); SI-B is the handout for Exercise 2 (frequency response); SI-C is the handout for Exercise 3 (component-sensitivity prediction); SI-D is the consolidated marking grid across the three exercises; SI-E gives the transistor-level realisation of the OTA block of Figure 1 together with a simulated characterisation of its state-controlled transconductance; SI-F records the differentiated second-year and third-year delivery tracks and the pre/post assessment instrument; and SI-G works all three exercises through to their deliverables (Supporting Information S1:

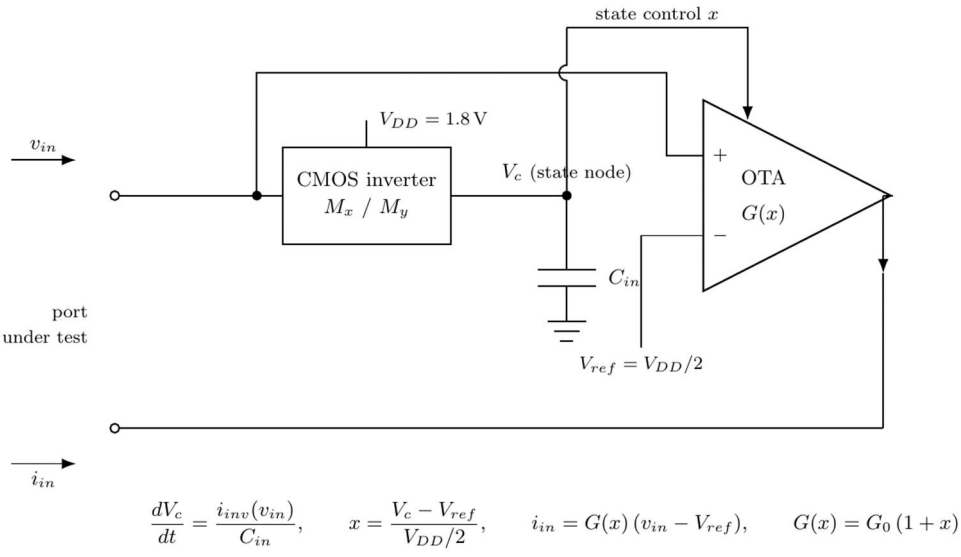


FIGURE 1 | Architecture of the adopted memristor emulator. The transistor-level realisation of the OTA block is given in Supporting Information S1: SI-E.

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Figures S3 and S4) as an exemplar full-credit submission and marking reference.

To the best of the author's knowledge, no prior open-source release combines these elements into a deploy-ready instructional package for the inverter–OTA memristor emulator. The remainder of this paper is organised as follows. Section 2 briefly reviews the constitutive relations defining a memristor and the experimental signatures that distinguish it from a non-linear resistor. Section 3 describes the adopted emulator topology, positions it relative to prior reports, and derives the first-order lobe-area relation. Section 4 describes the simulation methodology and justifies the choice of excitation band against the instrumentation of a typical undergraduate laboratory. Section 5 presents the simulation results, the frequency-sweep validation and the parametric validation of the first-order model. Section 6 summarises the three-session pedagogical module that wraps the simulation suite, its differentiation across year groups, a worked course-integration example, and an analysis of the procedural errors the assessment has to detect. Section 7 concludes.

2 | Memristor Fundamentals

Chua's original 1971 derivation showed that, by symmetry of the four basic two-terminal circuit variables—voltage v, current i, charge q, and flux linkage φ—a fourth element must exist, defined by a functional relationship between charge and flux:

$$\varphi = f(q) \tag{1}$$

Differentiating Equation (1) with respect to time and applying the elementary relations $dq/dt = i$ and $d\varphi/dt = v$ yields the port equation of a charge-controlled memristor:

$$v(t) = M(q(t)) \cdot i(t), \qquad M(q) = \frac{df}{dq} \tag{2}$$

Equation (2) makes explicit the defining property: the instantaneous resistance M depends on the integral of past current. For any non-trivial f, three experimental signatures necessarily follow when the device is driven by a periodic, zero-mean input [20]. (Equation (2) is the ideal-memristor case of the broader class of memristive systems formalised by Chua and Kang [21], to which the emulator studied here belongs.)

(S1) Pinched hysteresis: The Lissajous figure of $v(t)$ versus $i(t)$ is a closed curve passing through the origin ($i = 0 \Leftrightarrow v = 0$).

(S2) Frequency-dependent lobe collapse: As the excitation frequency $f_0 \to \infty$, the hysteresis lobe progressively shrinks toward a single-valued curve.

(S3) Lobe area scales monotonically with amplitude: For a fixed frequency, increasing the input amplitude widens the hysteresis lobe.

Any candidate memristor—fabricated or emulated—must reproduce these three fingerprints. The adopted emulator is validated against all three in Section 5: (S1) and (S2) in Sections 5.1 and 5.2, and (S3) as part of the parametric study of Section 5.3, which also supplies the quantitative target that students are asked to predict in Laboratory Exercise 3.

3 | Adopted Emulator Topology

Figure 1 shows the adopted emulator, identical in functional structure to the topology presented in Saxena [12], extended in Swaroop and Ahmad [13], implemented in inverter-fed form by Poornima (2024) [14], and most recently realised in a current-mode 13-transistor variant by Neifar et al. [15]. The circuit comprises three sub-blocks:

- Input stage: a complementary pair of MOS transistors (PMOS M_x, NMOS M_y, both with channel length $L = 1\,\mu$m; $W = 10$ and $5\,\mu$m, respectively) configured as a CMOS inverter. Driven by the input port voltage v_{in}, it acts as a transconductor that delivers a current $i_{\text{inv}}(v_{\text{in}})$ to the internal node V_c.
- Integrating capacitor $C_{\text{in}} = 22\,$nF, connected from V_c to ground. It performs a time integration of the inverter output current, so that V_c—equivalently, the normalised state variable $x = (V_c - V_{\text{ref}})/(V_{DD}/2)$ — plays the role of the internal state of Equation (2).
- State-modulated OTA whose transconductance is *controlled by the state node*, so that the current returned to the input port is

$$i_{\text{in}} = G(x)\,(v_{\text{in}} - V_{\text{ref}}), \qquad G(x) = G_0\,(1 + x), \qquad G_0 = 1\,\text{mS} \tag{3}$$

The supply rail is $V_{DD} = 1.8\,$V and V_{ref} is hard-tied to the mid-rail $V_{DD}/2 = 0.9\,$V. The MOSFETs are described by Level-1 models with $V_{TO} = \pm 0.7\,$V, $KP = 50\,\mu\text{A/V}^2$ (PMOS) and $100\,\mu\text{A/V}^2$ (NMOS), and channel-length modulation $\lambda = 0.02\,\text{V}^{-1}$.

Equation (3) is the structural feature that makes the circuit memristive rather than merely hysteretic, and it deserves emphasis because it is the point at which a naive implementation fails. The port current must be *proportional to the port voltage*, with the stored state modulating only the constant of proportionality. An OTA of fixed transconductance driven by V_c—that is, $i_{\text{in}} = g_m(V_c - V_{\text{ref}})$—produces a closed v–i loop that is hysteretic but is not pinched: its current at $v_{\text{in}} = V_{\text{ref}}$ is non-zero, so signature (S1) fails and the circuit behaves as a relay characteristic rather than as a memristor. In the topology adopted here, the capacitor voltage sets the OTA bias, and hence its transconductance; Supporting Information S1: SI-E gives a transistor-level realisation (Supporting Information S1: Figure S1) in which the tail device of a five-transistor OTA is gated by V_c, together with a simulated characterisation of the resulting $g_m(V_c)$ law (Supporting Information S1: Figure S2). Because $G(x)$ in Equation (3) is non-negative over the operating range, the emulated device is passive.

The use of an OTA as the current-delivering element of a memristor emulator predates the inverter-fed variants adopted here: Gül and Babacan [9] modelled a fabricated semiconductor memristor with an OTA-based circuit and corroborated it

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

experimentally, and the same port relation—a transconductance scaled by a stored state—underlies the topology used in this paper. A fabricated-device route is also available, and Babacan et al. [10] demonstrate it with a MOSFET-only circuit implementation of a semiconductor memristor; that route, however, presupposes the fabrication capability whose absence is the premise of this work.

The pedagogical economy of this topology is precisely the reason it was selected for the present teaching package: the CMOS inverter and the OTA are circuits a second-year student has already encountered in earlier modules, while the integrating capacitor is the simplest possible state-variable storage element. No exotic component—multiplier, sample-and-hold, switched-capacitor block—is introduced. The behavioural-level description of Equation (3) deliberately abstracts the OTA's transistor-level realisation; the student-facing focus is on the *system-level* relationship between the three sub-blocks and the resulting memristive port behaviour.

3.1 | First-Order Relation Between Component Values and Lobe Area

The single quantity a student can both predict on paper and measure on screen is the area enclosed by one lobe of the pinched hysteresis figure. Deriving it takes four steps and no calculus beyond a single integral, which makes it suitable as pre-laboratory preparation for the Analyse-level exercise of Section 6.

Step 1—the inverter as a transconductor: Biased at its mid-rail trip point, the CMOS inverter delivers a current to the state node that is, to first order, proportional to the port voltage:

$$i_{\text{inv}} \simeq -\, G_{m,\text{inv}}\,(v_{\text{in}} - V_{\text{ref}}), \qquad G_{m,\text{inv}} = g_{m,n} + g_{m,p} \tag{4}$$

For the Level-1 devices used here, $g_m = KP{\cdot}(W/L){\cdot}(V_{GS} - V_T)$ evaluates to 100 µS for each device at the trip point, so $G_{m,\text{inv}} = 200$ µS.

Step 2—the capacitor integrates it: With a sinusoidal excitation $v_{\text{in}} - V_{\text{ref}} = V_0 \sin \omega t$, integrating Equation (4) over C_{in} gives a state that lags the excitation by a quarter period:

$$x(t) = -\,X\cos\omega t, \qquad X = \frac{G_{m,\text{inv}}\,V_0}{(V_{DD}/2)\,\omega\,C_{\text{in}}} \tag{5}$$

X is the peak excursion of the normalised state. The quarter-period lag is the entire physical origin of the hysteresis: without it, G would be a single-valued function of v_{in} and the v–i locus would be a curve of zero area.

Step 3—the lobe area: Substituting Equations (3) and (5) into $A = \oint i\,dv$ and integrating over the half cycle for which $v_{\text{in}} \geq V_{\text{ref}}$, the constant term $G_0 v$ contributes nothing (it is single-valued) and the state-dependent term gives

$$A_{\text{lobe}} = \frac{2}{3} G_0 V_0^2 X = \frac{2}{3} \cdot \frac{G_0\,G_{m,\text{inv}}\,V_0^3}{(V_{DD}/2)\,\omega\,C_{\text{in}}} \tag{6}$$

Equation (6) is the result that the laboratory exercises are built around. It predicts four independent scaling laws—$A \propto f^{-1}$, $A \propto C_{in}^{-1}$, $A \propto G_0$ and $A \propto V_0^3$—each of which a student can verify in a few minutes of simulation. The f^{-1} dependence is signature (S2); the V_0^3 dependence is signature (S3) in quantitative form.

Step 4—the validity window: Equation (5) assumes the state stays inside its rails, $|x| \leq 1$. Setting $X = 1$ gives the lower edge of the usable excitation band:

$$f_{\text{min}} = \frac{G_{m,\text{inv}}\,V_0}{\pi\,V_{DD}\,C_{\text{in}}} \tag{7}$$

Below f_{min} the integrating capacitor saturates against the supply rails, the inverter degenerates into a comparator, and the emulator ceases to obey Equation (6). With the values adopted here, $f_{\text{min}} = 482$ Hz, so the 1–100 kHz band used throughout this paper sits entirely inside the valid region with better than a factor of two of margin at its lower edge. Equation (7) is also the design rule an instructor needs in order to move the demonstration band: C_{in} scales it inversely, so a laboratory that prefers a 100–10 kHz band simply raises C_{in} to 220 nF.

4 | Simulation Methodology

4.1 | Simulators and Source Files

The emulator is described by a single plain-text SPICE netlist. It was verified under:

- ngspice 44.2 (open-source), using emulator.cir directly;
- LTspice (proprietary but freely distributed by Analog Devices), using emulator_ltspice.net, which is the same file with the ngspice-specific. control/wrdata block replaced by a.tran directive—the circuit description itself is character-for-character identical.

The behavioural memductance of Equation (3) is expressed as a single non-linear current source,

```
Bota Vin 0 I = 1e-3*(1 + (V(Vc) - V(Vref))/0.9)*(V
(Vin) - V(Vref)),
```

a construct supported by both engines.

Cross-engine agreement was measured rather than assumed, because the claim that a student on either simulator obtains the same result is a claim the package has to earn. The 1 kHz reference run was executed in both engines and the final excitation period compared sample by sample on a common time grid: the largest deviation is 0.41% of full scale on v_{in}, 0.42% on V_c and 0.55% on i_{in}, and the derived observable—the single-lobe hysteresis area—agrees to 0.004% (30.1950 µV·A under ngspice against 30.1939 µV·A under LTspice). The residual per-sample difference is dominated by the differing internal time steps of the two solvers rather than by any difference in the circuit. The script check_ltspice_export.py in the repository performs this comparison automatically on an LTspice text export, so an

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

adopting instructor can repeat the check on their own installation in one command.

All numerical results reported below were produced with ngspice, which is preferred for batch experiments because it is controllable from the shell and integrates naturally with the post-processing pipeline.

4.2 | Excitation and Analysis Settings

The transient excitation in all experiments is a sinusoidal voltage centred at the mid-rail:

$$v_{\text{in}}(t) = 0.9 + V_0 \sin(2\pi f_0 t)\ V, \qquad V_0 = 0.3 \quad V, \qquad f_0 \in \{1, 10, 100\}\ \text{kHz} \tag{8}$$

Transient analysis uses the uic (use-initial-conditions) directive with 1000 time points per excitation period. Each run covers 200 full periods and only the final period is retained for analysis; this discards the start-up transient of the integrating node completely, which matters because the state node has no low-impedance DC path and its residual offset decays slowly. Post-processing is implemented in Python 3 with NumPy and Matplotlib (versions 1.26 and 3.8, respectively). Lobe areas are computed with the shoelace formula applied to the half of the closed contour for which $v_{\text{in}} \geq V_{\text{ref}}$; because a pinched hysteresis figure is a figure-of-eight whose two lobes are traversed in opposite senses, the signed area of the full contour is close to zero and must not be used as the observable—a point that is made explicitly in the student handout of SI-B.

4.3 | Why 1–100 KHz

The excitation band was chosen so that the module can be replicated on physical instrumentation without the simulation and the bench diverging, and the choice is worth stating explicitly because it constrains the design of the emulator through Equation (7).

A typical undergraduate electronics laboratory is equipped with a function generator of 5–25 MHz upper limit and an oscilloscope of 50–100 MHz bandwidth. The 1–100 kHz band, therefore sits at least one and a half decades below the generator's specified limit and between two and a half and five decades below the scope bandwidth, so neither instrument contributes appreciable amplitude or phase error, and neither probe capacitance (typically 10–15 pF) nor breadboard stray capacitance perturbs a 22 nF integrating node. The corresponding periods, 10 µs to 1 ms, fall in the middle of the time-base range of every teaching oscilloscope, and the band is low enough that the Lissajous figure can be produced directly in the instrument's X–Y mode rather than by post-processing—which is what allows a future hardware version of the module to be assessed with the same rubric as the simulated version. Finally, the port current amplitude over the band is 293–332 µA, which develops a 29–33 mV signal across a 100Ω series sense resistor: comfortably above the noise floor of a teaching oscilloscope, and small enough not to load the emulator. Frequencies above roughly 1 MHz were deliberately excluded: there, the lobe area falls below 0.03 µV·A, the hysteresis becomes invisible at any reasonable vertical scale, and the exercise would degenerate into reading a straight line.

4.4 | Portability Evidence

Table 1 claims that the package carries no deployment dependencies. That claim was tested rather than asserted, by running the complete pipeline on independent toolchains and comparing the observables the manuscript quotes (Table 2).

The two Python rows straddle the NumPy 1 → 2 major-version boundary, which is the API break most likely to affect a scientific script written today and run in 3 years' time; every printed digit is identical across it. Together with the LTspice row, this covers two operating systems, two simulators and two NumPy major versions. What is not covered, and should not be inferred, is macOS and older ngspice releases: the package has not been run there.

5 | Results and Discussion

5.1 | Pinched-Hysteresis Verification

Figure 2 shows the four canonical waveforms produced by the emulator under the 1 kHz case of the excitation of Equation (8): (a) the input port voltage $v_{\text{in}}(t)$ and the internal-state voltage $V_c(t)$, showing the quarter-period lag predicted by Equation (5); (b) the input port current $i_{\text{in}}(t)$; (c) the Lissajous figure v_{in} versus i_{in}, exhibiting the pinched-hysteresis lobes; and (d) the state-space orbit x versus v_{in}, which makes the lag directly visible as an open ellipse.

The pinch is exact rather than approximate. Measured over the final excitation period, the current at the $v_{in} = V_{ref}$ crossings is 7.5×10^{9} of the current amplitude—a number set by the numerical tolerance of the transient solver rather than by the circuit—so signature (S1) is satisfied identically. Over the same period, the memductance $G(x)$ sweeps from 0.500 to 1.500 mS, an ON/OFF ratio of exactly 3.00, and remains non-negative throughout, confirming that the emulated device is passive.

5.2 | Frequency-Dependent Lobe Collapse

Figure 3 plots the v–i Lissajous figure at the three excitation frequencies. The single-lobe areas are 30.20 µV·A at 1 kHz, 3.02 µV·A at 10 kHz and 0.30 µV·A at 100 kHz: the ratio between successive decades is 10.00 in both cases, so the lobe area falls by exactly one decade per decade of frequency, as Equation (6) predicts. At 100 kHz the trajectory has collapsed to within 1% of a single-valued straight line of slope G_0. This is signature (S2), and the fact that it is reproduced not merely qualitatively but with the exponent predicted from component values is what makes it usable as a graded laboratory observable.

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

TABLE 1 | Comparison of behavioural memristor emulators, including two representative designs from outside the inverter–OTA family.

Reference	Year	Topology family	Active blocks	Deployment dependencies	Source files released	Pedagogical package
Yu et al. [7]	2014	Floating, op-amp + multiplier	4 Op-amps + 2 multipliers	Analogue multiplier ICs (AD633 class); commercial SPICE for the macromodels	No	No
Koymen and Drakakis [11]	2014	Nanopower CMOS	6+	Foundry-calibrated CMOS process models	No	No
Babacan et al. [8]	2017	OTA-based, tunable	2 OTAs + multiplier	LM13700 or equivalent OTA plus multiplier; bench validation assumed	No	No
Gül and Babacan [9]	2018	OTA-based circuit model	1 OTA + multiplier	OTA plus multiplier IC; fabricated memristor for the corroboration	No	No
Babacan et al. [10]	2018	MOSFET-only, fabricated device	8 MOSFETs	Thin-film fabrication and characterisation facility	No	No
Saxena [12]	2018	CMOS inverter—OTA	3	Foundry CMOS process models	No	No
Swaroop and Ahmad [13]	2023	CMOS inverter—OTA + logic	3+	Commercial CMOS design environment	No	No
Poornima [14]	2024	Inverter-fed passive	2	Commercial CMOS design environment	No	No
Neifar et al. [15]	2025	Current-mode inverter—OTA	13 Transistors	Foundry CMOS process models	No	No
This work	2026	CMOS inverter—OTA (adopted)	3	None: free simulator (ngspice or LTspice), generic Level-1 models, no purchased IC, no fabricated device	Yes (shared netlist + Python)	Yes (3 differentiated exercises + rubric, MIT)

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

TABLE 2 | Cross-toolchain reproduction of the reported observables.

Operating system	Simulator	Python stack	Pinch residual	Lobe area at 1 kHz	Slope of A vs. f
Linux (kernel 6.12)	ngspice 44.2	CPython 3.13.12, NumPy 1.26.4, Matplotlib 3.10.9	7.47×10^{-9}	30.195 μV·A	−1.000
Linux (kernel 6.12)	ngspice 44.2	CPython 3.13.5, NumPy 2.2.4, Matplotlib 3.10.1	7.47×10^{-9}	30.195 μV·A	−1.000
Windows	LTspice	text export, checked with the released script	2.74×10^{-8}	30.194 μV·A	—

5.3 | Parametric Validation of the First-Order Model

Figure 4 tests Equation (6) against simulation along four one-at-a-time sweeps around the operating point of Section 4.2. The measured log–log slopes are −1.000 against frequency, −1.000 against C_{in},+1.000 against G_0 and +3.010 against V_0, versus the predicted −1, −1, +1 and +3. The residual is a constant 4.3% offset in magnitude across all four sweeps, consistent with the first-order estimate of $G_{m,\text{inv}}$ in Equation (4), neglecting the channel-length-modulation contribution to the inverter transconductance; because it is a constant prefactor, it does not affect any of the exponents, which are what the exercises ask students to predict.

The +3.010 slope of the amplitude sweep is signature (S3) in quantitative form, and it is a more demanding test than the usual qualitative statement that 'the lobe widens with amplitude': a cubic law is easy to distinguish from a linear or quadratic one on a log–log plot with four points, so a student's prediction can be marked objectively.

The scaling laws are not an artefact of the particular memductance law of Equation (3). Repeating the frequency sweep with a square-root law, $G \propto (V_c - V_T)^{1/2}$—the form that a real five-transistor OTA with its tail device in the triode region actually exhibits, as measured in SI-E—leaves the pinch exact and returns a log–log slope of −1.014 against frequency. This is expected: to first order in the state excursion, any monotonic non-negative $G(x)$ reproduces Equation (6) with only the prefactor changed. The robustness matters pedagogically, because it means an instructor who substitutes a different OTA model, or a student who eventually builds the circuit from discrete parts, will still measure the same exponents.

5.4 | Position Relative to Prior Reports

Table 1 places the present pedagogical package in context with nine representative memristor emulators and circuit models from the recent literature. Four of them—Saxena [12], Swaroop and Ahmad [13], Poornima [14] and Neifar et al. [15]—are the prior reports of the inverter–OTA topology adopted here. The remaining five come from outside that family, and are included so that the choice of the inverter–OTA route as the teaching vehicle can be judged rather than assumed: the floating relaxation-oscillator emulator of Yu et al. [7], the nanopower CMOS emulator of Koymen and Drakakis [11], the tunable OTA emulator with experimental verification of Babacan et al. [8], the OTA-based circuit model of Gül and Babacan [9], and the MOSFET-only implementation of a fabricated semiconductor memristor by Babacan et al. [10].

Several of those alternatives achieve higher fidelity than the design used here, and two of them— [8] and [10]—were validated against hardware rather than only in simulation. They pay for it in prerequisites. The op-amp and OTA designs [7–9] need an analogue multiplier and, in [7], a floating-port arrangement, none of which a second-year student has yet met; the CMOS designs [11–15] need foundry-calibrated process models or a commercial design environment; and [10] needs the thin-film fabrication and characterisation capability whose

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

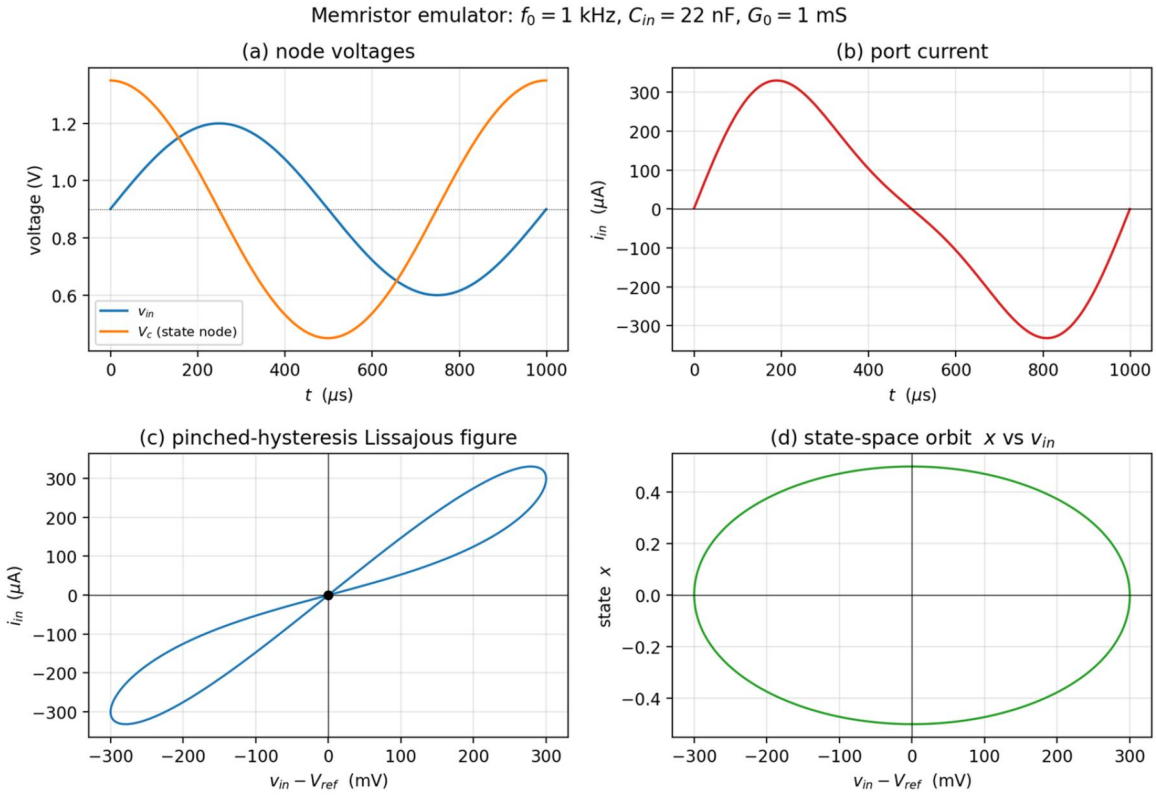


FIGURE 2 | Time-domain waveforms, pinched-hysteresis Lissajous figure and state-space orbit at $f_0 = 1$ kHz, $C_{\text{in}} = 22$ nF, $G_0 = 1$ mS. (a) Node voltages: input port voltage v_{in} and internal-state voltage V_c, showing the quarter-period lag. (b) Input port current i_{in}. (c) Pinched-hysteresis Lissajous figure, v_{in} versus i_{in}; the black marker is the origin. (d) State-space orbit, normalised state x versus v_{in}.

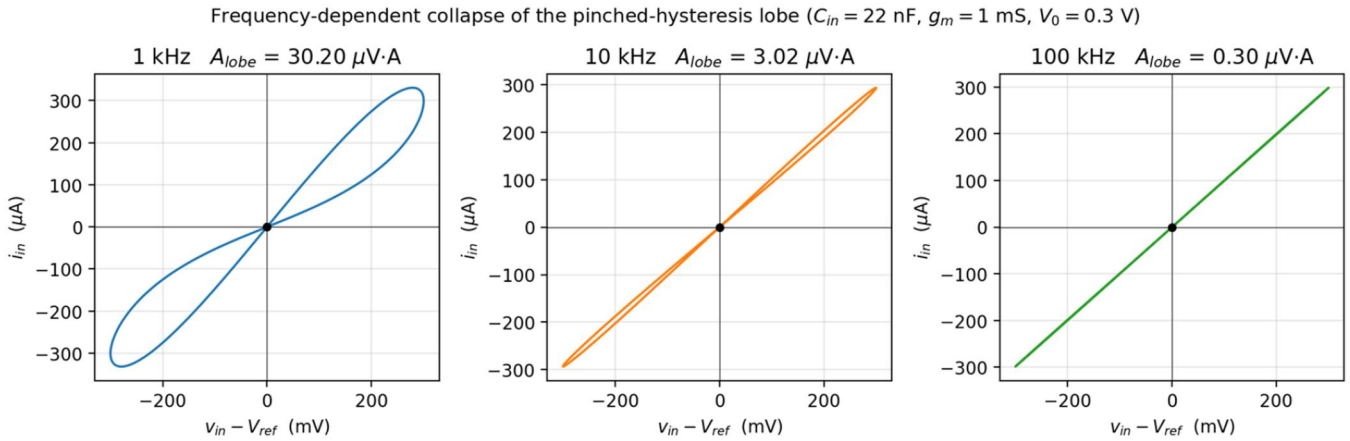


FIGURE 3 | Frequency-dependent collapse of the pinched-hysteresis lobe at 1, 10 and 100 kHz. The lobe area falls by a factor of 10.00 per decade of frequency.

absence is the premise of this paper. The 'Deployment dependencies' column records exactly this, and is the practical reason the inverter–OTA family was selected: of the nine prior designs, none can be run by a department that owns only a free simulator and a general-purpose computer.

6 | Pedagogical Application

The simulation suite supports a three-session laboratory module of total duration ≈6 contact hours, mappable to the ECTS workload of a single instructional unit in a second- or third-year analogue electronics course. The three exercises are summarised in Table 3; full student handouts, with worked examples, marking rubrics and timestamps, are provided as Supporting Information S1: SI-A, SI-B and SI-C, with the consolidated marking grid in Supporting Information S1: SI-D.

The progression deliberately follows an ascending Bloom-taxonomy gradient—a framework whose continued utility for assessing engineering-student competency levels has been reaffirmed by Ullah et al. [22] —so that students begin by *reproducing* an instructor-provided simulation (remember/understand), then *modify* the excitation parameters and observe

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

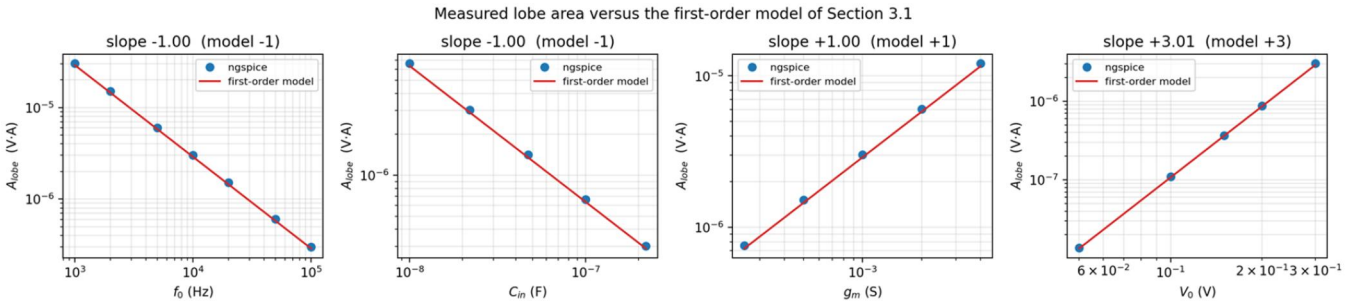


FIGURE 4 | Validation of Equation (6). Markers are ngspice measurements; lines are the closed-form prediction. Fitted log–log slopes are printed above each panel.

TABLE 3 | Three-session pedagogical module summary.

Session	Exercise	Bloom level	Duration	Pre-simulation analytical work
1	Hysteresis fingerprint	Remember/understand	90 min	None
2	Frequency-response sweep	Apply	90 min	Stepwise frequency selection
3	Component-sensitivity prediction	Analyse	120 min	Required, timestamped

the consequence (Apply), and finally *predict-then-verify* the response of the emulator to two component-value perturbations (Analyse). The terminal exercise carries the highest cognitive load because the prediction is required *before* any simulation is run, with the prediction document timestamped—a constraint that prevents post-hoc rationalisation and forces engagement with Equation (6).

6.1 | Targeted Learning Outcomes

By the end of the three-session module, a student is expected to be able to:

- (LO1) **Identify** the memristive fingerprint of an unknown two-terminal device from its v–i Lissajous trajectory under sinusoidal excitation;
- (LO2) **Operate** an open-source SPICE simulator (ngspice) and a proprietary one (LTspice) to reproduce identical transient behaviour from a shared netlist;
- (LO3) **Modify** simulator excitation parameters (frequency, amplitude) and predict the resulting change in lobe area;
- (LO4) **Derive** the first-order relation of Equation (6) between component values (C_{in}, G_0) and observable port behaviour, and use it to obtain a numerical prediction;
- (LO5) **Reflect** on the discrepancy between an analytically-derived prediction and a SPICE-verified observation, and propose a refinement of the first-order model.

LO1 and LO2 are exercised in Sessions 1–2; LO3–LO5 are exercised in Session 3. The marking rubric in SI-D is aligned with these outcomes one-to-one.

6.2 | Differentiation Across Year Groups

The same three exercises are delivered along two tracks, because the prerequisite knowledge of a second-year cohort that has just completed a basic circuits course differs substantially from that of a third-year cohort that has already taken an integrated-circuits course. The two tracks share all source files, all figures and the same total contact time; they differ in what is given to the student and what the student is asked to produce. Table 4 records the difference, and the full paired handouts are given in Supporting Information S1: SI-F.

6.3 | Course-Integration Example

To make the deployment concrete, the module is specified here as it is intended to be inserted into a real course rather than as an abstract template. The host course is a second-semester analogue electronics course carrying 5 ECTS, of which the laboratory component is 2 ECTS (≈ 50–60 total student hours). The module occupies three consecutive weekly laboratory sessions in the second half of the semester, after the sessions on the MOS transistor and the RC integrator, on which it depends, and before the session on non-linear amplifiers.

Per student, the workload is six contact hours plus approximately 4 h of preparation and report writing, that is, about 0.4 ECTS, or one-fifth of the laboratory component. No timetable change is required beyond substituting three existing sessions, and no procurement is required at all: the software is free, and the department needs only the computers it already uses for its circuit-simulation sessions.

The compute budget inside those sessions was measured rather than estimated, by timing each released command on an ordinary laptop (single core, no GPU). The Exercise 1 simulation takes 0.69 s and its plotting script 1.21 s; the three-frequency sweep of Exercise 2 takes 1.96 s plus 1.13 s of plotting, and the five-frequency version used in the worked solution of SI-G (Supporting Information S1: Figure S3) takes 11.1 s in total. Regenerating every figure in this paper, including the 21-run parametric study of Section 5.3 and the 46-run OTA characterisation of SI-E, takes 24.5 s. The released source is 52 kB—

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

TABLE 4 | Differentiation of the module across year groups.

Aspect	Second-year track (after basic circuits)	Third-year track (after integrated circuits)
Inverter treatment	Given as a black-box transconductor with $G_{m,\mathrm{inv}}$ stated	Student computes $G_{m,\mathrm{inv}}$ from KP, W/L and the trip-point overdrive
Equation (6)	Supplied; student uses it	Derived by the student from Equations (3)–(5) as pre-laboratory work
Exercise 2 deliverable	Qualitative statement that the lobe shrinks with frequency	Log–log lobe-area plot with a fitted exponent and its uncertainty
Exercise 3 prediction	Direction of change only (larger/smaller/unchanged)	Numerical prediction with a stated tolerance band
Validity window, Equation (7)	Stated as a given operating constraint	Derived, and used to re-target the band for a specified C_{in}
OTA realisation (SI-E)	Not used	Read and related to the behavioural law; optional transistor-level re-simulation
Typical marking emphasis	LO1–LO3	LO3–LO5

Note: The second-year variant is deliverable immediately after a first course in circuit analysis, because it requires only the notions of a controlled source, a capacitor as an integrator, and a Lissajous figure. The third-year variant requires MOS small-signal analysis and is where Equation (6) becomes a derivation rather than a given.

TABLE 5 | Anticipated student errors, their measured consequence at the 1 kHz reference point, and the assessment response.

Error	What the student does	Measured consequence	Assessment response
E1	Applies the shoelace formula to the whole closed contour rather than to one lobe	1.6×10^{-4} μV·A instead of 30.195 μV·A, that is, 5×10^{-6} of the correct value: the figure-of-eight cancels and the student concludes there is no hysteresis at all	Pre-empted by an explicit warning box in the SI-B handout and by the released lobe_area() helper; a report showing no closed lobe at the lowest frequency scores 0
E2	Analyses the first excitation period instead of the last, keeping the start-up transient	−8.5% at 1 kHz, but below 0.3% at every higher frequency; the fitted log–log slope moves only from −1.0000 to −0.9845	Not caught by the slope criterion, which admits -1.0 ± 0.1. SI-B, therefore, now carries an explicit steady-state checkpoint requiring both windows to be reported and the choice justified
E3	Runs below the validity edge of Equation (7)—here 300 Hz against $f_{\mathrm{min}} = 482$ Hz	Equation (6) predicts 100.65 μV·A, the simulation gives 61.35 μV·A, an over-prediction of 39%, with the state excursion at $\lvert x\rvert\max = 0.998$ against its limit of 1	This is the assessed content of Exercise 3, in the milder form of case P4 (worked solution in Supporting Information S1: Figure S4); the score-2 criterion requires the student to evaluate f_{min} and reach the diagnosis

Note: E2 is the reason this analysis was worth doing. The error is large enough to matter at the frequency where the hysteresis is most visible, yet it perturbs the fitted exponent by less than the tolerance the rubric was originally written with—so a student could make it, report a slope of −0.98, and be marked correct. Measuring the consequence exposed the gap, and the SI-B rubric was changed in response. An assessment instrument that has not been tested against the errors it is supposed to detect is an assumption, not an instrument.

a 41-line netlist and 510 lines of Python—so the only non-trivial resource is disk: one raw transient output at the sampling density used here is 19 MB, which is worth knowing before 30 students each write several of them to a shared network drive. In practice, no session is compute-bound, and the contact time is spent where it is intended to be spent, on interpretation rather than on waiting. Session 1 runs in a computer laboratory with one workstation per pair of students; Sessions 2 and 3 can be run as supervised open-laboratory time because each student works from the same shared netlist. Assessment contributes to the laboratory portion of the course mark through the SI-D grid.

The transfer cost to another institution is the reason the package is released under a permissive licence rather than described: an adopting instructor downloads the repository, runs ngspice −b emulator.cir followed by python3 plot_results.py to confirm the toolchain, prints SI-A to SI-C, and is ready to teach. The only site-specific decision is which of the two tracks of Section 6.2 to run, and—if the local laboratory prefers a different excitation band—the single value of C_{in} that Equation (7) fixes.

6.4 | Anticipated Student Errors and What the Rubric Does About Them

Three procedural errors are available to a student working through this module, and each was reproduced deliberately in order to measure what it does to the reported number. Table 5

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

records them. They are not hypothetical: each is a step a careful student can take for a defensible reason.

6.5 | Limitations of the Present Study

The present paper stops at the design and validation of the pedagogical package and does not report classroom deployment data. Its claims are therefore of two kinds, and the distinction should be read carefully. The claims about the artefact—that the emulator satisfies (S1)–(S3), that the lobe area obeys Equation (6), that the package runs on free software—are established by the simulations reported in Section 5 and are reproducible from the released files. The claims about learning—that the Bloom-aligned progression and the predict-then-verify constraint of Exercise 3 produce deeper engagement than symbolic-only instruction—are not established here. They rest on the deliberate instructional design of the exercises and on the established literature on simulation-based learning, and they remain to be tested.

A formal evaluation is accordingly planned: a pre/post concept inventory administered around the three sessions, the rubric distribution of SI-D as a secondary measure, and a comparison against a cohort taught the same content symbolically. The instrument is given in SI-F so that other institutions can administer the identical measure and pool results; the package is released now under MIT precisely so that such data can be gathered in more than one place. Until that evidence exists, the contribution claimed here is a validated and freely deployable teaching artefact, not a demonstrated learning gain.

7 | Conclusion

This paper has presented an open-source pedagogical packaging of the standard CMOS-inverter + integrator + OTA memristor emulator topology—a topology already established in the research literature since 2014 and most recently reported in 2025. The contribution is the combination of a single shared SPICE netlist that runs under both a free and a proprietary simulator, a Python post-processing pipeline, a closed-form first-order model relating component values to the observable hysteresis lobe area, three Bloom-aligned laboratory exercises differentiated across 2 year groups with assessment rubrics and worked exemplar solutions, and an MIT-licensed public release.

Over the 1–100 kHz band the package reproduces all three of Chua's signatures quantitatively: the v–i locus is pinched at the origin to within 10^{-8} of the current amplitude, the lobe area collapses as f^{-1} at a measured slope of −1.000, and it grows as V_0^3 at a measured slope of +3.010, with the closed-form model of Equation (6) tracking the measurements to a constant 4.3% across four independent parameter sweeps. The emulator is built from textbook sub-blocks already familiar to second-year electronics students, and the excitation band was chosen to match the instrumentation of an ordinary undergraduate laboratory so that the module can later be replicated in hardware without redesign.

The complete package—netlists, post-processing scripts, figures, the seven Supplementary Information documents and the assessment instrument — is available under the MIT License at https://github.com/proffatih/memristor-emulator-teaching-suite.

Author Contributions

Fatih Gül: conceptualisation, methodology, software, validation, formal analysis, investigation, writing – original draft, writing – review and editing, visualization.

Acknowledgements

The author thanks the Artificial Intelligence and Internet of Things Research Laboratory at Recep Tayyip Erdoğan University for providing the computing infrastructure on which the simulations were performed. The author used Anthropic Claude for prose polishing and for assistance with the Python post-processing and simulation-driver scripts. All simulation results, numerical values and figures were generated by the author using ngspice and were verified by the author, who reviewed and edited all output and takes full responsibility for the content.

Funding

The author has nothing to report.

Conflicts of Interest

The author declares no conflicts of interest.

[REDACTED — public repository URL provided in title page]

By releasing all source files publicly, the suite removes the principal practical barrier—no fabricated device available—that has so far kept memristive concepts out of the undergraduate laboratory. Future extensions will add memcapacitor and meminductor variants of the same minimal-component philosophy— electronically controllable floating memcapacitor circuits of the kind reported by Gür et al. [23] provide a natural starting point—and a hardware version built from a discrete CMOS inverter array and a commercial OTA, assessed with the same rubric.

Data Availability Statement

All materials are publicly available at https://github.com/proffatih/memristor-emulator-teaching-suite under the MIT License.

References

1. L. Chua, "Memristor—The Missing Circuit Element," *IEEE Transactions on Circuit Theory* 18, no. 5 (September 1971): 507–519, https://doi.org/10.1109/TCT.1971.1083337.

2. D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found," *Nature* 453, no. 7191 (May 2008): 80–83, https://doi.org/10.1038/nature06932.

3. H.-S. P. Wong, H. Y. Lee, S. Yu, et al., "Metal-Oxide RRAM," *Proceedings of the IEEE* 100, no. 6 (June 2012): 1951–1970, https://doi.org/10.1109/JPROC.2012.2190369.

4. M. Hu, C. E. Graves, C. Li, et al., "Memristor-Based Analog Computation and Neural Network Classification With a Dot Product Engine," *Advanced Materials* 30, no. 9 (2018): 1705914, https://doi.org/10.1002/adma.201705914.

5. G. Indiveri, B. Linares-Barranco, T. J. Hamilton, et al., "Neuromorphic Silicon Neuron Circuits," *Frontiers in Neuroscience* 5 (May 2011): 73, https://doi.org/10.3389/fnins.2011.00073.

6. G. S. Rose, J. Rajendran, N. McDonald, et al., "Hardware Security Strategies Exploiting Nanoelectronic Circuits," *in 18th Asia and South*

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, 2013, 368–372, https://doi.org/10.1109/ASPDAC.2013.6509623.

7. D. Yu, H. Iu, A. L. Fitch, and Y. Liang, "A Floating Memristor Emulator Based Relaxation Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers* 61, no. 10 (2014): 2888–2896, https://doi.org/10.1109/TCSI.2014.2333687.

8. Y. Babacan, A. Yesil, and F. Kacar, "Memristor Emulator With Tunable Characteristic and Its Experimental Results," *AEU–International Journal of Electronics and Communications* 81 (November 2017): 99–104, https://doi.org/10.1016/j.aeue.2017.07.012.

9. F. Gul and Y. Babacan, "A Novel OTA-Based Circuit Model Corroborated by an Experimental Semiconductor Memristor," *Microelectronic Engineering* 194 (July 2018): 56–60, https://doi.org/10.1016/j.mee.2018.03.012.

10. Y. Babacan, A. Yesil, and F. Gul, "The Fabrication and MOSFET-Only Circuit Implementation of Semiconductor Memristor," *IEEE Transactions on Electron Devices* 65, no. 4 (April 2018): 1625–1632, https://doi.org/10.1109/TED.2018.2808530.

11. I. Koymen and E. M. Drakakis, "CMOS-Based Nanopower Memristor Dynamics Emulator," *in 2014 14th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA)*, 2014, 1–2, https://doi.org/10.1109/CNNA.2014.6888637.

12. V. Saxena, "A Compact CMOS Memristor Emulator Circuit and Its Applications," *in 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018, 173–176, https://doi.org/10.1109/MWSCAS.2018.8624008.

13. V. Swaroop and Z. Ahmad, "Design of CMOS Memristor Emulator and Logic Gates for Neuromorphic Circuits," *in 2023 International Symposium on Devices, Circuits and Systems (ISDCS)*, 2023, 1–4, https://doi.org/10.1109/ISDCS58735.2023.10153559.

14. G. Poornima, "Inverter Fed Passive Memristor Emulator," *in 2024 5th International Conference on Circuits, Control, Communication and Computing (I4C)*, 2024, https://doi.org/10.1109/I4C62240.2024.10748465.

15. A. Neifar, I. Barraj, H. Mestiri, and M. Masmoudi, "Design of a Current-Mode OTA-Based Memristor Emulator for Neuromorphic Medical Application," *Micromachines* 16, no. 8 (August 2025): 848, https://doi.org/10.3390/mi16080848.

16. A. J. Magana and T. de Jong, "Modeling and Simulation Practices in Engineering Education," *Computer Applications in Engineering Education* 26, no. 4 (2018): 731–738, Jul, https://doi.org/10.1002/cae.21980.

17. M. S. N. Alnassar, "Utilization of Open-Source Software in Teaching the Physics of P-N Diodes," *Computer Applications in Engineering Education* 31, no. 4 (2023): 867–883, Jul, https://doi.org/10.1002/cae.22611.

18. D. Omidvarkarjan, M. Hofelich, J. Conrad, C. Klahn, and M. Meboldt, "Teaching Agile Hardware Development With an Open-Source Engineering Simulator: An Evaluation," *Computer Applications in Engineering Education* 31, no. 4 (July 2023): 946–962, https://doi.org/10.1002/cae.22616.

19. S. Gürkan, M. Karapınar, H. Sorgunlu, O. Öztürk, and S. Doğan, "Development of a Photovoltaic Panel Emulator and LabVIEW-Based Application Platform," *Computer Applications in Engineering Education* 28, no. 5 (September 2020): 1291–1310, https://doi.org/10.1002/cae.22302.

20. L. Chua, "If It's Pinched It's a Memristor," *Semiconductor Science and Technology* 29, no. 10 (2014): 104001, https://doi.org/10.1088/0268-1242/29/10/104001.

21. L. O. Chua and K. Sung Mo Kang, "Memristive Devices and Systems," *Proceedings of the IEEE* 64, no. 2 (February 1976): 209–223, https://doi.org/10.1109/PROC.1976.10092.

22. Z. Ullah, A. Lajis, M. Jamjoom, A. Altalhi, and F. Saleem, "Bloom's Taxonomy: A Beneficial Tool for Learning and Assessing Students' Competency Levels in Computer Programming Using Empirical Analysis," *Computer Applications in Engineering Education* 28, no. 6 (November 2020): 1628–1640, https://doi.org/10.1002/cae.22339.

23. M. Gur, F. Akar, K. Orman, Y. Babacan, A. Yesil, and F. Gul, "Electronically Controllable Fully Floating Memcapacitor Circuit," *Circuits, Systems, and Signal Processing* 42, no. 11 (November 2023): 6481–6493, https://doi.org/10.1007/s00034-023-02448-6.

Supporting Information

Additional supporting information can be found online in the Supporting Information section.
Supporting File: cae70283-sup-0001-supplementary_information.pdf.

10990542, 2026, 6, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/cae.70283 by Recep Tayyip Erdoan Üniversitesi, Wiley Online Library on [09/11/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License